



PTO/SB/21 (09-04)

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**TRANSMITTAL
FORM**

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission

9

Application Number

10/722,686

Filing Date

November 24, 2003

First Named Inventor

Benware, Robert

Art Unit

2819

Examiner Name

Le, Don P.

Attorney Docket Number

03-1122

ENCLOSURES (Check all that apply)

Fee Transmittal Form



Fee Attached



Amendment/Reply



After Final



Affidavits/declaration(s)



Extension of Time Request



Express Abandonment Request



Information Disclosure Statement



Certified Copy of Priority Document(s)

Reply to Missing Parts/
Incomplete ApplicationReply to Missing Parts
under 37 CFR 1.52 or 1.53

Drawing(s)



Licensing-related Papers



Petition

Petition to Convert to a
Provisional Application

Power of Attorney, Revocation



Change of Correspondence Address



Terminal Disclaimer



Request for Refund



CD, Number of CD(s) _____

☐ Landscape Table on CD

Remarks

- Issue Fee Payment



After Allowance Communication to TC

Appeal Communication to Board
of Appeals and InterferencesAppeal Communication to TC
(Appeal Notice, Brief, Reply Brief)

Proprietary Information



Status Letter

Other Enclosure(s) (please identify
below):

1. Power of Attorney and Correspondence
Address Indication Form, PTO/SB/81
2. Statement Under 37 CFR 3.73(b),
PTO/SB/96
3. Return Postcard

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name

LSI Logic Corporation

Signature

Printed name

Sandeep Jaggi

Date

9/20/05

Reg. No.

43,331

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature

Typed or printed name

Mark Salvatore

Date

9-21-05

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :

Robert Benware

Serial No. :

10/722,686

Filed :

November 24, 2003

For :

Self-Timed Scan Circuit for ASIC
Fault Testing

Group Art Unit :

2819

Examiner :

Le, Don P.

Atty Docket :

81631 / 03-1122

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date below:

Mark Salvatore

September 21, 2005 *Mark Salvatore*

Date

Signature

SUBMISSION OF FORMAL DRAWINGS PURSUANT TO 37 C.F.R. §1.85

Official Draftsman

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby substitutes the enclosed formal drawings for those presently in the above referenced application.

LSI Logic Corporation
1621 Barber Lane, MS D-106
Milipitas, CA 95035
408-433-7475

Date: 9/20/05

Respectfully submitted,

Sandeep Jaggi

Sandeep Jaggi

Reg. No. 43,331